

(19)



JAPANESE PATENT OFFICE

Ref. no. 4

## PATENT ABSTRACTS OF JAPAN

(11) Publication number: **60110060 A**

(43) Date of publication of application: 15 . 06 . 85

(51) Int. Cl.

G06F 13/00  
H04L 13/00

(21) Application number: 58219226

(22) Date of filing: 21 . 11 . 83

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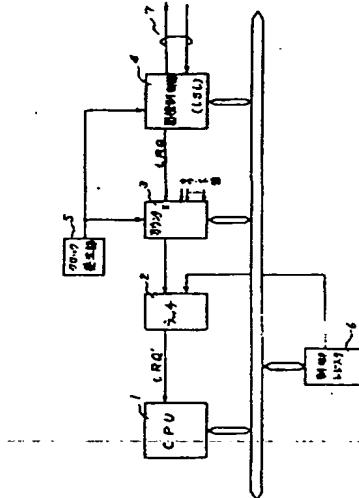
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**(54) DATA TRANSMISSION CONTROL SYSTEM**

(57) Abstract:

**PURPOSE:** To reduce the load and to improve the data processing efficiency with a data transmission control system by using a delay means to inform that 2 transmission buffers empty to a processor by a single interruption.

**CONSTITUTION:** When the transmission is through with characters set to a unit transmission buffer, a circuit control part 4 activates an interruption signal IRQ showing the end of transfer of a character. Then a counter 3 counts the circuit clocks supplied from a clock generating part 5. The count output is turned into an interruption signal to be applied to a CPU1 through a latch 2. Then the latch 2 is reset via a control register 6 and at the same time the next transmission data is written to two transmission buffers of the part 4. In such a way, the transmission interrupting frequencies to the CPU1 are considerably reduced and therefore improve the data processing efficiency.



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